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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,277	07/08/2003	Thomas R. Bednar	BUR920020092US1	1276

30449 7590 07/28/2005

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EXAMINER
TAT, BINH C

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,277	BEDNAR ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/604277 filed on 07/08/03.

Claims 25-42 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 25-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Bedmar et al. (U.S Patent 2004/0060023).

4. As to claims 21, and 31, Bedmar et al. disclose an electrical structure comprising: a parent terrain denoted as V0 (see fig 1, fig 3 and fig 5 element 111 paragraph 0029); and N voltage islands denoted as V1, and V2 said voltage island V1 nested within said parent terrain V0 and said voltage island V2 nested within said voltage island V1 (see fig 1, fig 3, and fig 5 paragraph 0034, and paragraph 0042 to 0050).

5. As to claims 22, and 32, Bedmar et al. disclose wherein each voltage island of the N voltage island includes one or more voltage power supplies selected from the group consisting of an internal voltage island VDDI power supply, an externally supplied state saving VDDSS power supply, an externally supplied VDDN power supply, and combinations thereof (see fig1 and fig 3 paragraph 0028 to 0029).

6. As to claims 23, and 33, Bedmar et al. disclose wherein said one or more power supplies of voltage island Vx for Xr--zl, 2,..,. N are each independently coupled to one of (a) said one or more power supplies of voltage island Vv. for Y=1, 2,..., N, X not equal to Y, (b) a VDDO power supply of said parent terrain or (c) one or more external to said parent terrain power supplies (see fig 1, fig 3, and fig 5 paragraph 0034, and paragraph 0042 to 0050).

7. As to claims 24, and 34, Bedmar et al. disclose wherein each voltage island of the N voltage islands includes (a) an externally supplied VDDN power supply and a voltage shifting means, or (b) said externally supplied VDDN power supply and a fencing means or (c) said externally supplied VDDN power supply, said voltage shifting means and said fencing means (see fig 1, and fig3 paragraph 0027-0032).

8. As to claims 25, and 35, Bedmar et al. disclose wherein said fencing means comprises logic latches (see fig 1 paragraph 0033).

9. As to claims 26, and 36, Bedmar et al. disclose wherein each voltage island of the N voltage islands further includes one or more substructures selected from the group consisting of (a) an internal voltage island VDDI power distribution network, (b) state saving means, (c) one or more switching elements coupled between said externally supplied VDDN power supply and said internal voltage island VDDI power distribution network, and (d) one or more voltage buffering circuit (see fig 1, and fig3 paragraph 0027-0032).

10. As to claims 27, and 37, Bedmar et al. disclose wherein said one or more switching elements is selected from the group consisting of hard connections, voltage regulators headers and footers (see fig 1, and fig3 paragraph 0027-0032 and background).

11. As to claims 28, and 38, Bedmar et al. disclose wherein said state saving means includes at least one state saving latch (see fig 1 paragraph 0033).

12. As to claims 29, and 39, Bedmar et al. disclose wherein one or more voltage islands of the N voltage islands further includes a power management state machine coupled to an internal voltage island VDDI power supply distribution network, said power management state machine of voltage island Vx for X=1, 2,. . ,, N located in (a) voltage island Vv for Y=1, 2...., N, Y less than X, or (b) in said parent terrain (see fig 1, fig 3, and fig 5 paragraph 0034, and paragraph 0042 to 0050).

13. As to claims 30, and 40, Bedmar et al. disclose wherein said parent terrain is an integrated circuit chip or a voltage island within said integrated circuit chip (see fig1 and fig 3 paragraph 0028 to 0029).

14. As to claims 41, and 42 Bedmar et al. disclose further including: additional voltage islands denoted as V3, V4, ... Vn, a voltage island Vz nested within a voltage island Vz-1 for Z = 3, 4,....., N, wherein N is an integer of at least 3 (see fig 1, fig 3, and fig 5 paragraph 0034, and paragraph 0042 to 0050 and background).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BINH TAT
Art Unit 2825
July 22, 2005

Paul Dinh